

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Leon Zheng et al.  
Application No. : 10/783,789 Confirmation No. : 7188  
Filed : February 20, 2004  
For : FLEXIBLE ACCUMULATOR IN DIGITAL SIGNAL  
PROCESSING CIRCUITRY  
Art Unit : 2193  
Examiner : Chat C. Do

New York, New York 10036  
August 18, 2009

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

PRE-APPEAL-BRIEF REQUEST FOR REVIEW

Sir:

Applicants request review of the Final Office Action dated July 27, 2009. No amendments are being filed with this Request, which is being filed with a Notice of Appeal.

**Concise Argument for Which Review is Being Requested** begins on page 2 of this Pre-Appeal-Brief Request for Review.

**REMARKS**

**Summary of Office Action**

Claims 1-10 were pending in the above-identified patent application.

Claims 1-10 have been finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. U.S. Patent No. 4,876,660 (hereinafter "Owen") in view of Simkins et al. U.S. Patent Application Publication No. 2005/0144215 (hereinafter "Simkins").

**Applicants' Claimed Invention**

Applicants claimed invention is generally directed to methods for initializing or zeroing an accumulator value with minimal latency. As recited by applicants' independent claim 1, a first pair of input signals and a second pair of input signals are routed to circuitry that is concentrated in a particular area of a programmable logic resource. For example, the input signals may be routed to one or more multiplier-accumulator blocks. A multiply operation is applied to the second pair of input signals using the circuitry. A feedback output, which is initially set to zero, is applied to the circuitry. The first pair of input signals is concatenated. The feedback output is concatenated onto the end of the concatenated first pair of input signals. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating of the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

As recited by applicants' independent claim 8, a pair of input signals is routed to circuitry that is concentrated in a particular area of a programmable logic resource. A multiply operation is applied to the pair of input signals using the circuitry. A register is cleared in the circuitry based on at least one dedicated configuration bit that is set. A feedback output, which is initially set to zero, is applied to the circuitry. The feedback output is concatenated onto the end of the contents of the register. An accumulate operation is then applied to a result of the multiply operation and a result of the

concatenating the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

#### The References

Owen refers to a fixed-point multiplier-accumulator architecture. *See* Owen, Abstract. Owen's FIG. 6A shows a functional block diagram of an emmitter-coupled logic (ECL) multiplier-accumulator. *See* Owen col. 7, 47-61; col. 9, ll. 19-61; and FIG. 6A.

Simkins refers to a field-programmable gate array (FPGA) with a number of cascading digital signal processing (DSP) slices. The DSP slices may be used for multiple mathematical operations. *See* Simkins, Abstract. Simkins' FIG. 3C shows a schematic of a DSP slice. Simkins' FIG. 14 shows a FPGA having DSP slices. Simkins' FIG. 17 shows a DSP slice that carries out multiply and add operations.

#### Clear Error in the Rejection

The Examiner acknowledges that Owen does not disclose concatenating the feedback output onto the end of the concatenated first pair of input signals (Office Action, page 3). The Office Action also acknowledges that Owen does not disclose concatenating the feedback output onto the end of the contents of a register (Office Action, page 5). However, the Office Action contends that Simkins shows both of these features in figures 3C, 14, paragraphs [0121]-[0122] and paragraph [0217], and that it would have been obvious to modify Owen to include these features from Simkins (Office Action, page 3 and page 5). Applicants respectfully disagree and submit that neither Owen nor Simkins, alone or in combination, show applicants' claimed concatenating.

The only concatenating shown in Simkins' figure 3C and discussed in paragraphs [0121]-[0122] is the concatenating of the 18-bit outputs of registers BREG 360 and AREG 362 to form 36-bit output A:B to be sent to multiplexer 370 and which may be sent to adder/subtractor 382. At no point, however, does figure 3C or paragraphs [0121]-[0122] show or suggest concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals as recited by applicants'

independent claim 1. Simkins also fails to show or suggest concatenating the feedback output (which is initially set to zero) onto the end of the contents of a register as recited by applicants' independent claim 8. The concatenation of the outputs of two registers is not the same as concatenating a feedback output, which is initially set to zero, onto the end of the concatenated first pair of input signals (claim 1) or onto the end of the contents of a register (claim 8). The Examiner further contends that paragraph [0122] shows the concept for placing a zero signal at the end of a concatenated first input pair of signals (Office Action - Response to Arguments, page 6). Applicants respectfully disagree. In Simkins' figure 3C and paragraphs [0121]-[0122] the addition of a number represented by a first number of bits with the number zero, represented by a second, larger number of bits, would still produce a resulting number represented by leading zero bits at its beginning. This is different than concatenating a feedback output onto the end of a concatenated first pair of input signals (claim 1) or onto the end of the contents of a register (claim 8).

Figure 14 of Simkins also does not show or suggest concatenating the feedback output onto the end of the concatenated first pair of output signals (claim 1) or concatenating the feedback output onto the end of the contents of the register (claim 8). Rather, figure 14 shows a FPGA having DSP slices. The FPGA has a 36-bit concatenation bus, A:B, on which the high-order 18 bits convey an operand A, and the remaining bits convey an operand B. As such, it is clear that although the concatenation bus may convey 36 bits of concatenated information, this bus, by itself, performs no concatenating as recited by applicants' claims 1 and 8. Additionally, nothing in figure 14 shows concatenating the feedback output (initially set to zero) onto the end of the concatenated first pair of input signals (claim 1) or onto the end of the contents of a register (claim 8).

Simkins paragraph [0218] discusses that the least significant bit (LSB) of a bit string is located at the end of the bit string. Simkins, paragraph [0217] discusses a 36-bit concatenation of operands, A:B, being input into multiplexing circuitry 1721 shown in figure 17 via an input bus. The input bus can be "sign extended or zero filled as appropriate to 48 bits." The Examiner contends that this shows the step of concatenating as is defined in applicants' claims 1 and 8 (Office Action, page 3 and page 7). Applicants respectfully submit that sign extending or zero filling a 36 bit input bus to be 48 bits is

different than the claimed feature of "concatenating the feedback output onto the end of the concatenated first pair of input signals" as recited by applicants' amended independent claim 1. Sign extending or zero filling a 36 bit input bus to be 48 bits is also different than the claimed feature of "concatenating the feedback output onto the end of the contents of the register" as recited by applicants' amended independent claim 8. In particular, one of ordinary skill in the art would understand that sign-extending or zero-filling a 36-bit number to be 48 bits, where the LSB is at the end of the 48 bits, would produce a result with 12 zero bits at the beginning of the 36-bit number. This is different than concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals (claim 1) or onto the end of the contents of a register (claim 8).

For at least the foregoing reasons, applicants submit that independent claims 1 and 8 are patentable. None of the cited references, alone or in combination, show or reasonably suggest applicants' claimed concatenating as recited by these independent claims. Dependent claims 2-7, 9, and 10 are allowable for at least the same reasons. Applicants respectfully request, therefore, that the rejections of claims 1-10 be withdrawn.

### Conclusion

Applicants respectfully submit that this application, including claims 1-10, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,

/Brian E. Mack/

---

Brian E. Mack  
Reg. No. 57,189  
Attorney for Applicants  
ROPES & GRAY LLP  
Customer No. 36981  
1211 Avenue of the Americas  
New York, New York 10036-8704  
Tel.: (212) 596-9000